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Control of InGaAs and InAs facets using metal modulation epitaxy

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Control of faceting during epitaxy is critical for nanoscale devices. This work identifies the origins of gaps and different facets during regrowth of InGaAs and InAs adjacent to patterned features. Molecular beam epitaxy near SiO_2 or SiN_x led to gaps, roughness, or polycrystalline growth, but low-arsenic metal modulated epitaxy produced smooth and gap-free (001) planar growth up to the gate. The resulting self-aligned field effect transistors (FETs) were dominated by FET channel resistance rather than source–drain access resistance. Higher As_2 fluxes led first to conformal growth, then pronounced {111} facets sloping up away from the mask. © *2015 American Vacuum Society*.
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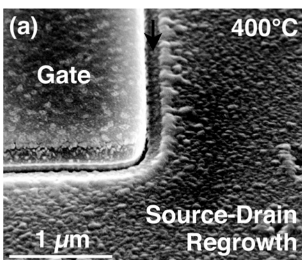
I. INTRODUCTION

Nanoscale devices have many advantages, including high bandwidth and packing density. But the gate oxide in Si based metal–oxide–semiconductor (MOS) field effect transistors (FETs) has become difficult to shrink, leading to short-channel effects and off-state leakage currents. Further improvement in FET performance could come from semiconductors with higher carrier velocities. InGaAs and other III–V materials have electron velocities 5–10 times higher than those in silicon, producing strong interest in III–V MOSFETs.[1–5] Significant progress has been made on dielectrics and interface control layers for III–V channels, and scalable CMOS-like process flows have been demonstrated.[6] But high source/drain resistances have hindered device performance. Contacts are challenging because III-V semiconductors lack an equivalent to the highly conductive salicides used for Si CMOS, although reacted contacts[7] and NiInAs (Ref. 8) have shown contact resistances below $10^{-8}\ \Omega\ \mathrm{cm}^{-2}$.

Source/drain resistance also results from heterojunction barriers, long distances, and low carrier densities, in addition to contact resistance.[9] Even with doped channels for depletion-mode FETs, the typical distances between metal and device introduce parasitic access resistance, which impairs high frequency operation.[10] Making the contacts self-aligned would greatly reduce access resistance without requiring critical lithographic alignment.[11] Self-aligned dopant implants in III-V materials lack the necessary active carrier concentrations (above $2 \times 10^{19}\ \mathrm{cm}^{-3}$) to prevent source exhaustion in thin channels at CMOS current densities.[12–14] Self-aligned, selective growth is commonly reported for metalorganic MBE and chemical beam epitaxy.[15,16] But these have generally focused on regrowth of larger bandgap binaries such as InP rather than low-resistance contacts, and may include growth temperatures that are incompatible with high-k dielectrics on III-V channels.

We previously demonstrated regrowth of highly doped InGaAs contacts by molecular beam epitaxy (MBE), but these showed either gaps (absence of growth) or polycrystalline regrowth near gate masks, as shown in Fig. 1. The resulting FET source resistances were $R_s = 0.5$–$5\ \mathrm{M}\Omega\ \mu\mathrm{m}$, leading to poor MOSFET performance.[17] Also, the gap size depended on mesa width: shorter gate lengths (narrower mesas) with $L_g < 500\ \mathrm{nm}$ produced slightly smaller gaps in regrowth. Similar self-aligned MBE InGaAs regrowth for tunnel FETs showed difficulty in the control of facets near the mask, and an unexplained moat or gap was apparent near



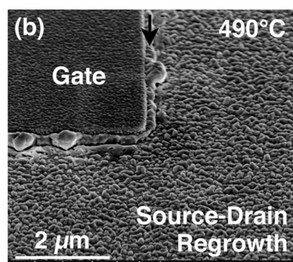


Fig. 1. Top view SEM of MBE regrowth near a SiO_2-masked gate. Note 200 nm gap in regrowth near gate at low growth temperatures near 400 °C (a), and polycrystalline growth at ≥490 °C (b).

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several devices, wider than the gate overhang, similarly reported by Chun.[18]

One possible explanation for this difficulty is a local change in the ratio of group V to group III atom species on the surface. The III/V ratio can greatly affect surface kinetics during epitaxial growth and promote formation of different facets near step edges or raised features such as FET gates. Shen and Nishinaga reported from microprobe reflection high energy electron diffraction (RHEED) analysis that for all InAs growth temperatures, increased arsenic flux led to faster growth on the (111)A plane, producing a flat (001) surface,[19] but the reverse was true near (111)B facets on GaAs.[20] This work studied the mechanisms controlling regrowth next to patterned features in order to prevent gaps and control adjacent facet angles.

II. EXPERIMENT

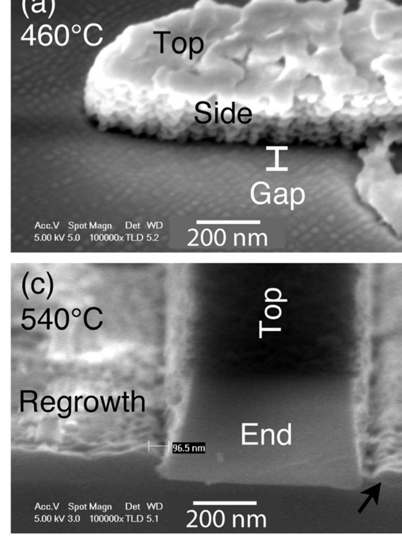
To be specific, we examined the origin of gaps, roughening, and faceting in the regrowth of InGaAs near a SiO_2 mask, with or without SiN_x sidewalls that fully encapsulated a FET metal gate. Two sets of samples were patterned on InGaAs lattice matched to InP, then verified by fabricating FETs. Transmission length methods (TLMs) far from device features did not accurately measure resistance of regrown InGaAs near FET gates,[17,21] so all samples in this work used a FET-like geometry.

All regrowths were performed in an Intevac Mod Gen II MBE using a valved arsenic cracker. Growth temperatures were measured using a Modline 3V pyrometer calibrated by k-Space Associates BandiT band edge thermometry. Before regrowth, each patterned sample was exposed to UV ozone for 20 min to remove trace organics and form a sacrificial oxide. It was then dipped in 1:10 $HCl:H_2O$ for 60 s, followed by a 60 s rinse in deionized water. The wafer was immediately loaded into ultrahigh vacuum and baked at 200 °C overnight. The wafer was then exposed to thermally cracked H_2 at 1×10^{-6} Torr for 30 min at 420 °C as measured by noncontact thermocouple, with occasional rotation to assure uniform exposure of H from various angles. RHEED showed a clear (2×4) reconstruction at 200 °C before the regrowth began, indicating a nominally clean surface.

The first set used simple SiO_2 masks (dummy gates) followed by migration enhanced epitaxy (MEE)[22–27] for source/drain regrowth, to attempt to fill the gaps observed in Fig. 1. SiO_2 masks were patterned by photolithography, and then the wafer was cleaned as above and loaded for regrowth. Group III fluxes were $In = 9.7 \times 10^{-8}$ and $Ga = 5.1 \times 10^{-8}$ Torr for $T_{sub} \leq 540$ °C. Above $T_{sub} > 540$ °C, In fluxes were increased to compensate for In desorption, calibrated by x-ray diffraction (XRD). As shown in Fig. 2, MEE growth quality improved at higher temperatures, with no gaps near masks, fewer pinholes, and less crosshatching. But facets persisted near masks, and access resistance was 7.7 kΩ μm.[21]

The second set of samples used metal modulation epitaxy (MME, Fig. 3)[28] to force longer and more uniform surface migration regardless of distance from mask. MME is similar to periodic supply epitaxy (PSE)[29] but with lower As_2 flux to ensure high group III surface mobility. Since it is necessary to reproduce the geometry, strain, and other local conditions near actual FETs,[17] this set used a complete MOSFET gate stack as detailed in Ref. 17, including Al_2O_3 high-*k* dielectric and metal gate. The metal was covered by patterned SiO_2 and encapsulated in conformal 20–30 nm SiN_x sidewalls. The Al_2O_3 high-*k* was etched by dilute KOH, exposing the InGaAs surface for regrowth, leaving the SiO_2, SiN_x, and newly exposed InGaAs intact. The processed wafers were then cleaned and loaded for regrowth as above.

The MME consisted of group III deposition for 3.8 s to grow approximately 2 monolayers of InGaAs, followed by a 15 s pause under the same constant As_2 flux. This cycle was repeated 80 times to grow 40 nm of InGaAs. The pyrometer reading did not change during the cycle. Unlike traditional MEE at low temperature, the arsenic flux was not interrupted,



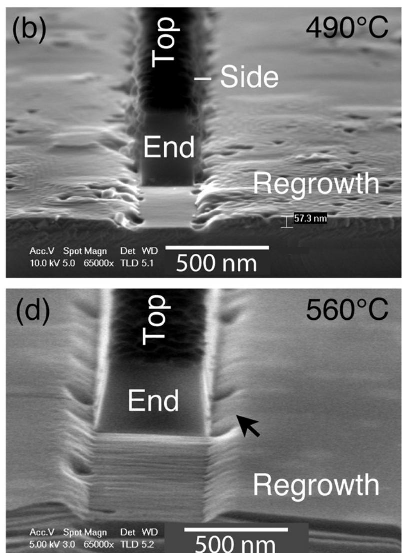


Fig. 2. Oblique side (a) and cleaved face [(b)–(d)] SEM views of MEE regrowth near SiO_2 dummy gates, at different growth temperatures. Above 490 °C, regrowth showed no gaps and fewer pinholes, but facets (arrows) persisted near gates.

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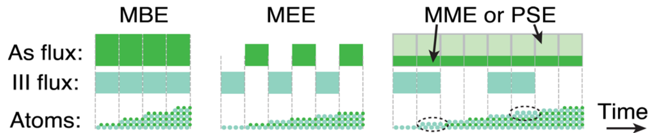

FIG. 3. (Color online) Typical flux timing diagrams for MBE, MEE, MME, and PSE, and cross section of growth surface at each step. Squares represent ~1 monolayer. The V/III flux ratio is ≫1 in MBE and PSE, ~1 in MEE, and <1 in MME. III-on-III (circled) has very high surface mobility for group III adatoms.

since InGaAs would decompose at these temperatures. Total InGaAs group III fluxes (beam equivalent pressure) were 1.5×10^{-7} Torr. Silicon doping was provided simultaneous with each group III pulse, corresponding to a doping level of $[Si] = 8 \times 10^{19}\,cm^{-3}$ and $n = 5 \times 10^{19}\,cm^{-3}$ for metal contact resistivities[30] $R_c \leq 2\ \Omega\ \mu m^2$. In contrast with the polycrystalline InGaAs in Ref. 17, R_c here was small enough to be neglected for all samples in this work, verified by transmission line methods (TLM) far from FET gates. Arsenic fluxes were 5.6×10^{-7}, 1.0×10^{-6}, 2×10^{-6}, and 5×10^{-6} Torr for the respective InGaAs layers, ending with conditions similar to those in Fig. 2(d). Marker layers of 20 nm $In_{0.52}Al_{0.48}As$ were grown by conventional MBE with an As_2 flux of 5×10^{-6} Torr. Substrate temperatures were decreased from 540 °C to 500 °C during the InAlAs layers, ensuring a smooth and conformal surface and freezing the surface profile of the underlying InGaAs for later analysis. InAlAs lattice matching was verified by XRD measurements of blanket InAlAs films grown under similar conditions. No extra pauses were used before or after the InAlAs, in order to prevent surface profile changes from annealing. The InAlAs was also doped with $[Si] = 8 \times 10^{19}\,cm^{-3}$.

RHEED showed a continuous (4 × 2) pattern during the first three InGaAs layers, indicating a group III-rich surface. It did not change during the arsenic-only steps, nor from one InGaAs layer to the next, although it did revert to a conventional (2 × 1) pattern during the InAlAs layers. RHEED during the fourth InGaAs layer, with highest As_2 flux, oscillated between group III rich (4 × 2) during the group III pulses and group V rich $\beta 2(2 \times 4)$ during the pauses. RHEED during the InAlAs layers was initially spotty with substrate temperatures near 540 °C, but it became streaky again as substrate temperatures approached 500 °C, indicating a smooth surface.

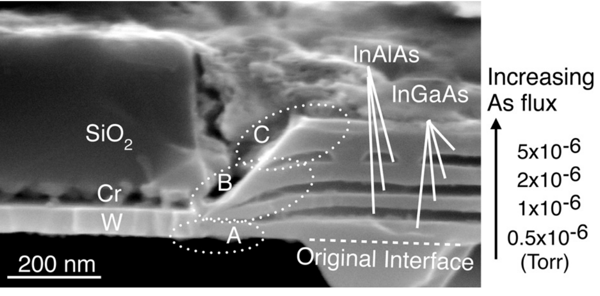

FIG. 4. Cross section SEM of InGaAs:Si layers grown with increasing As fluxes, separated by InAlAs marker layers. (A) Lowest arsenic flux shows complete (001) planar growth without gaps near gate or SiO_2/SiN_x. (B) Conformal growth. (C) Complete {111} faceting. The conformal SiN_x sidewall over the SiO_2, Cr, and W is not visible at this resolution. Debris on top was due to sample preparation process.

Figure 4 shows a scanning electron microscopy (SEM) of the sample after FIB cross section. A brief stain etch using dilute HCl was used to distinguish InGaAs from InAlAs. InGaAs with the lowest As_2 flux (5×10^{-7} Torr) filled the entire (001) plane right up to the mask. Higher As_2 fluxes produced a tapered and conformal layer, with no further fill along the gate sidewall. The highest As_2 fluxes (5×10^{-6} Torr) produced growth terminated by {111} planes sloping up away from the mask. InAlAs layers also showed some thinning next to the mask due to shadowing of source material by the tall gate stack and off-normal MBE cell geometry. There was no visible pileup near the (001)/{111} step edges, which indicates high Ga/In surface mobility on the (001) facet. There was no visible selectivity between (111)A and (111)B surfaces, which we interpret as an indication of fully group III rich surfaces. We observed no significant differences in facet angles for masks aligned along (110) or $(1\bar{1}0)$. A constant average RHEED intensity suggested there was no Ga droplet formation, and no droplets were visible in SEM.

To verify these results and also test them with InAs, which makes low resistance n-type contacts, we fabricated actual FETs. Source/drain regrowth of a single 50 nm layer of either $In_{0.53}Ga_{0.47}As$ or relaxed InAs was done by MME using $As = 5 \times 10^{-7}$ Torr, then capped with *in-situ* molybdenum and processed into FETs as in Ref. 17. On-state resistance versus gate length for the InAs-regrown FETs is plotted in Figs. 5(a) and 5(b). The R_{on} data showed that unlike earlier devices, the access resistance (extrapolation to $95 \pm 50\ \Omega\ \mu m$ at $L_g = 0$) was now a small fraction of total on-state resistance, 600 Ω μm. Total on-state resistivity R_{on} was 600 Ω μm for $L_g = 200$ nm and InAs contacts, so source and drain resistances are below 50 Ω μm each. Figure 5(c) shows good filling next to the mask for both InAs despite strain relaxation, little to no faceting, and little growth on gate sidewalls. Similar InGaAs growth showed a partial (100) growth followed by a short, shallow slope. MME regrowth of InAs using a higher As_2 flux of 2×10^{-6} Torr showed high-angle slopes in SEM (not shown), possibly [111] facets.

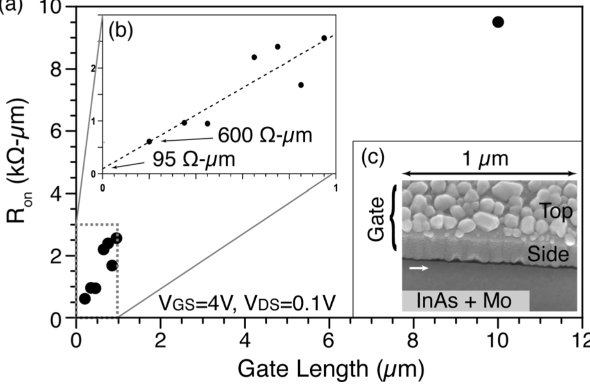

FIG. 5. (a) Total on-state resistance vs gate length (mask finger width) L_g for InGaAs channel FETs with regrown InAs contacts. (b) Expanded view of (a). Dashed line is fit over 0.2–1.0 μm, extrapolated to $R_{sd} \approx 95\ \Omega\ \mu m$ at $L_g = 0$. (c) Off-normal SEM view of region near gate (white arrow) after InAs MME regrowth and Mo deposition.

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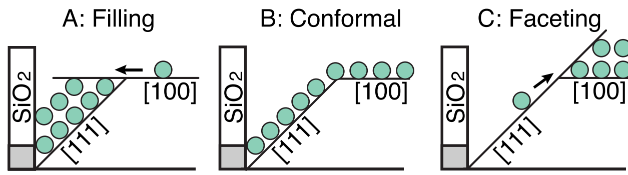

FIG. 6. (Color online) Surface mobility affects facet competition. Planes with high surface mobility suffer a net loss of atoms to planes with stronger bonds. Cases A-C correspond to conditions observed in Fig. 3.

III. DISCUSSION

We interpret these results as follows. Facet competition occurs when adatoms can move from one facet to another, as shown in Fig. 6. The facet with higher surface mobility generally has weaker bonds and loses atoms to its neighbor. From another perspective, the residence time for group III adatoms is longer on a slow-diffusion surface, providing more time for additional atoms to arrive and bond them in place. Thus, the facet with low surface mobility grows thicker but not wider. The facet with high surface mobility gets wider but not thicker as atoms move to a neighboring facet.[31] Smooth, low-index facets suggest a negligible or negative Schwoebel barrier.

The gaps in regrowth next to surface features can be explained by two separate effects, both based on local changes in the III/V ratio. First, the incorporation mechanisms of As and Ga/In are different. In and Ga tend to migrate on the growth surface, while As tends to evaporate and be replaced.[32] During growth, tall features (gates) block some As_2 flux from surrounding areas, while Ga and In continue to migrate until reaching areas with higher As_2 flux. Second, at growth temperatures much above 400 °C, In and Ga tend to bond relatively weakly on SiO_2 or SiN_x, so they can readily migrate to neighboring semiconductor. As with shadowing, the III/V ratio is increased locally, as shown in Fig. 7. This mechanism explains the sensitivity to gate length (mask width), since a larger mask area can provide more Ga and In atoms, up to the limit of the surface diffusion length of Ga and In on the dielectric.

Low-As MME prevented both gaps and {111} faceting by strongly increasing the group III surface coverage, and therefore surface mobility, at all distances from the mask. As shown in Fig. 3, MME alternates between strongly As-rich and III-rich conditions. Regions farther from the gate no longer acted as a sink for group III adatoms since diffusion rates were similar everywhere.

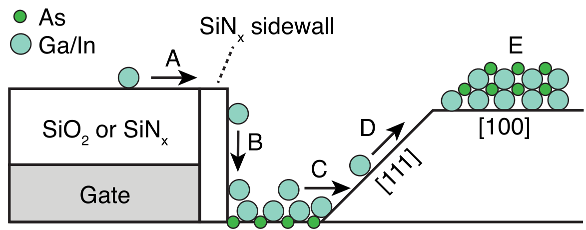

FIG. 7. (Color online) Gap mechanism. (A) Weak adhesion of In and Ga on SiO_2 leads to migration to neighboring semiconductor surface. (B) Arriving Ga/In atoms locally enrich the III/V ratio, leading to rapid surface diffusion (C). As the III/V ratio decreases farther from gate, growth begins on low-index facets (D) and eventually becomes planar and As-terminated (E).

Shen and Nishinaga reported that decreased As flux led to migration of atoms from the (001) surface to (111)A planes during InAs growth.[19] This led to the (001) plane growing wider and {111} planes becoming less pronounced. The opposite was reported for GaAs near (111)B facets.[20] In contrast, we find that an increased arsenic flux increased faceting of both (111)A and (111)B, and the best gap-free fill next to dielectric-coated features occurred with the lowest arsenic flux. We note there are multiple differences between our growth conditions and Shen's, such as higher growth temperatures, group III-rich pauses for migration enhancement, high Si doping, and As_2 rather than As_4.

We did not observe cusps in the regrowth. We attribute this to sufficiently high surface mobility on the (001) surface under all conditions, so adatoms did not pile up near the {111}-(001) intersections but instead diffused uniformly over the surface. Hata reported that Ga has a surface diffusion length of 1–8 μm on GaAs at somewhat higher temperatures (560 °C),[33] and In has an even higher surface mobility than Ga. The lack of a visible cusp sets a lower bound on (001) surface mobility of about 3 μm.

Nucleation and growth on the mask, visible in Fig. 2(a), could change local growth conditions over the course of the growth. The first InGaAs layer could have excess group III atoms migrating from the SiO_2 cap to the semiconductor surface, but once nucleated, InGaAs on top of the mask would consume group III. However, previously reported devices showed faceting with or without selective growth.[34] Although Fig. 4 shows growth on the sides of the mask, other samples did not; yet, they all showed similar faceting next to masks.

The total on-state resistivity places an upper bound of 300 Ω μm on source and drain resistivities. Actual resistivities are likely much lower than this, but scatter in the data precludes a confident extrapolation to $L_g = 0$. Even so, this on-state resistance is an order of magnitude better than our previous enhancement-mode MOSFETs.[17]

Finally, we note that the thinning of InAlAs near the mask is insufficient to explain InGaAs faceting. Single layers of InGaAs grown without InAlAs showed the same faceting under similar stoichiometry, such as in Fig. 2(d) and "C" in Fig. 4. Also, Fig. 4 clearly shows conformal, nonfaceting InGaAs for $[As] = 10^{-6}$ Torr even though the underlying InAlAs already has a wedge profile. This rules out InAlAs as the cause of [111] faceting.

IV. SUMMARY AND CONCLUSIONS

We found that varying growth temperature in both MBE and MEE of InGaAs on InP was insufficient to provide flat, high quality surfaces without gaps near dielectric masks including SiO_2 and SiN_x. Low temperatures left gaps, attributed to a local enhancement of the III/V ratio due to migration of In and Ga from the mask, and possibly shadowing of As by tall features (e.g., FET gate) during growth at lower temperatures. High growth temperatures created rough and defective material near the mask, possibly due to differences in surface mobility of Ga versus In atoms, leading to In-rich growth and strain relaxation.

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On the other hand, MME enabled uniform surface mobility and homogeneous growth across the whole wafer, including areas near dielectric masks. Pulses of 2 monolayers of group III atoms were grown under metal-rich conditions, followed by an As_2 soak to consume the excess group III atoms. MME eliminated gaps and pinholes and enabled self-aligned regrowth with no crosshatching.

Varying the As_2 flux in MME also allowed control of the facets adjacent to dielectric features such as gate sidewalls. High As_2 fluxes produced well-defined {111} planes. Fluxes closer to stoichiometry, marked by alternating (2×4) and (4×2) RHEED patterns with each growth cycle, led to conformal growth. Such facet control is important for self-aligned contacts and nanoscale self-assembled devices. Finally, a gap-free (001) planar growth up to the gate was achieved when the As_2 flux was roughly half that necessary to produce alternating RHEED patterns. MOSFETs with MME regrown InAs source/drain were no longer limited by access resistance, which was $95 \pm 50\ \Omega\ \mu$m, but by channel resistance. The facet control presented here opens new device possibilities by offering, for example, shaped sacrificial layers for T-gates, while preserving the high active doping density offered by MBE.

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